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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,058	04/08/2004	Takehiro Suzuki	1035-505	7339

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,058	SUZUKI, TAKEHIRO	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/08/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

2. Figures 7(a, 7(b), 8 and 9 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 10 is objected to because of the following informalities: line 4, the CDV' should read 'CVD' (chemical vapor deposition). Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 6-7, 10 are rejected under 35 U.S.C. 102(b) as being anticipated by US Pub 2002/0043723 to Shimizu et al.

Regarding claim 1, Shimizu discloses a semiconductor device in fig. 1, comprising: a semiconductor substrate 1 having formed thereon a semiconductor element 20; a first wiring layer 2 [0093] formed on said semiconductor substrate 1 at above an operating region (gate, source/drain) where said semiconductor element 20 is formed, said first wiring layer 2 being electrically connected to said operating region, fig. 1; a second wiring layer 7 [0093] formed on said semiconductor substrate 1 at above said first wiring layer 2; and a bonding pad 14 to be electrically connected to an external connection terminal [0093] formed on said semiconductor substrate 1 at above said second wiring layer 7, fig. 1, at least a part of said bonding pad 14 being located right above said operating region, wherein said second wiring layer 7 includes a plurality of wirings 107(a-b), fig. 1, formed in the region right under said bonding pad 14, a predetermined wiring 7a [0101] of said plurality of wirings 7a-b is connected to said bonding pad 14, fig. 1, and an insulating film 8 [0103] is formed between other wirings 7b than the predetermined wiring 7a among said plurality of wirings 7a-b, and the bonding pad 14; said other wirings 7b provided parallel to the edges of said

bonding pad 14 are not formed in regions right under the edges; and said insulating film 8 is made up of an inorganic insulating film only [0124].

Regarding claim 6, Shimizu discloses the semiconductor device as set forth in claim 1, wherein said bonding pad 14 is to be electrically connected to said inner lead by an inner lead bonding process, and said other wirings 7b formed parallel to the edges of a region to be electrically connected to an inner lead on a surface of said bonding pad 14 are not formed in regions right under the edges [0148] fig. 1.

Regarding claim 7, Shimizu discloses a semiconductor device in fig. 1 comprising: a semiconductor substrate 1 having formed thereon a semiconductor element 20; a first wiring layer 2 formed on said semiconductor substrate 1 at above an operating region (gate, source/drain) where said semiconductor element 20 is formed, said first wiring layer 2 being electrically connected to said operating region; a second wiring layer 7 formed on said semiconductor substrate 1 at above said first wiring layer 2; and a bonding pad 14 to be electrically connected to an inner lead by an inner lead bonding process [0148], formed on said semiconductor substrate 1 at above said second wiring layer 7, at least a part of said bonding pad 14 being located right above said operating region, wherein said second wiring layer 7 includes a plurality of wirings 7a-b formed in the region right under said bonding pad, a predetermined wiring 7a of said plurality of wirings is connected to said bonding pad 14, and an insulating film 8 is formed between other wirings 17b than the predetermined wiring 17a among said plurality of wirings, and the bonding pad 14; said other wirings 7b provided parallel to edges of said bonding pad are not formed in regions right under the edges of the

regions electrically connected to the inner lead on the surface of said bonding pad, fig. 1; and said insulating film 8 is made up of an inorganic insulating film only [0124].

Regarding claim 10, Shimizu discloses the semiconductor device as set forth in claim 1, wherein said insulating film 8 is made up of a silicone oxide film and a silicone nitride film, formed by the CVD [0124].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-5, 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pub 2002/0043723 to Shimizu et al in view of Applicant Admitted Prior Art (APA).

Regarding claims 2-3, 8-9 Shimizu discloses the semiconductor device as set forth in claim 1, wherein said other wirings 7b are not formed beyond the edge of the bonding pad 14, fig.1, said other wirings 7b being provided parallel to the edges of bonding pad 14 and the bonding pad in under stress by inner bonding process [0148] and [0150].

But Shimizu does not expressly discloses the in expanded regions right under said expanded regions as expanded with a stress in a process of electrically connecting said bonding pad to an external connection terminal,

wherein respective lengths of the expanded regions in the expanding direction of said bonding pad are set to fall in a range of from 2 micron to 3 micron.

However, APA discloses in fig. 9 a semiconductor device comprises a wire 202 having bonding pad 201, an expanded regions right under said expanded regions 201a-b as expanded with a stress in a process of electrically connecting said bonding pad to an external connection terminal 208, fig. 9, wherein respective lengths of the expanded regions in the expanding direction of said bonding pad 201 are set to fall in a range of from 2 micron, see background of the invention in fig. 9.

At the time the invention was made; it would have been obvious to one of ordinary skill in the art to conclude that the bonding pad 14 of Shimizu would have the expanded regions as claimed. Where the claimed and the prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Regarding claims 4-5, Shimizu does not disclose the semiconductor device as set forth in claim 2, wherein: said bonding pad and said external connection terminal are electrically connected by the chip-on-glass or chip-on board.

However, APA discloses the semiconductor device wherein bonding pad 201 and said external connection terminal are electrically connected by the chip-on-glass (COG) or TCP, see background of the invention. At the time the

invention was made; it would have been obvious to one of ordinary skill in the use the teaching of APA with Shimizu for intended use because the recitation 'chip-on-glass' or 'chip-on-board' of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.

Regarding claim 11, Shimizu discloses a semiconductor device in fig. 1, comprising: a semiconductor substrate 1 having formed thereon a semiconductor element 20; a first wiring layer 2 formed on said semiconductor substrate 1 at above an operating region where said semiconductor element 20 is formed, said first wiring layer 2 being electrically connected to said operating region; a second wiring layer 7 formed on said semiconductor substrate 1 at above said first wiring layer 2; and a bonding pad 14 to be electrically connected to an external connection terminal [0093], formed on said semiconductor substrate 1 at above said second wiring layer 7, at least a part of said bonding pad 14 being located right above said operating region, wherein said second wiring layer 7 includes a plurality of wirings 7a-b, a predetermined wiring 7a of said plurality of wirings is connected to said bonding pad 14, and an insulating film 8 is formed between other wirings 7b than the predetermined wiring 7a among said plurality of wirings, and said bonding pad 14; said other wirings 7b are formed so as to avoid regions right under the edges in the lengthwise direction of said bonding pad 14 to 3 micron outside the regions; and said insulating film includes an inorganic insulating film [0124].

But Shimizu does not expressly disclose 3 micron outside the region.

However, Shimizu clearly discloses no second wire layer 7b right under the edge and outside of the bonding pad 14. Therefore, the distance from the edge of the bonding pad 14 to the outside would have been approximately within the range as claimed in the micron or sub micron structure wherein the thickness of the wire 7a-b are about 7 micron [0186].

Regarding claim 12, Shimizu discloses the semiconductor device as set forth in claim 11, wherein said insulating film 8 is made up of an inorganic insulating film only [0124].

Regarding claim 13, Shimizu discloses the semiconductor device as set forth in claim 11, wherein at least a part of said other wirings 7b is formed in a region right under said bonding pad 14, and other wirings 7b formed in the region right under the bonding pad 14 are formed only in a region right under a region electrically connected to an inner lead [[0147] on a surface of said bonding pad, fig. 20.

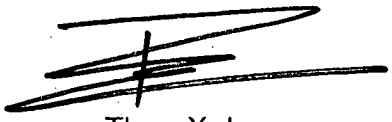
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
Patent Examiner
02 June 2005